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5 Novel fault-tolerant techniques for high capacity RAMs

Chih-Hsien Hsu; Shyue-Kung Lu; Sy-Yen Kuo;

Dependable Computing, 2001. Proceedings. 2001 Pacific Rim International Symposium on , 17-19 Dec. 2001

Pages:11 - 18

[\[Abstract\]](#) [\[PDF Full-Text \(844 KB\)\]](#) IEEE CNF

6 An eight-bit prefetch circuit for high-bandwidth DRAM's

Sunaga, T.; Hosokawa, K.; Nakamura, Y.; Ichinose, M.; Igarashi, Y.;

Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 1 , Jan. 1997

Pages:105 - 110

[\[Abstract\]](#) [\[PDF Full-Text \(1012 KB\)\]](#) IEEE JNL

7 Fault-tolerant designs for 256 Mb DRAM

Kirihata, T.; Watanabe, Y.; Hing Wong; DeBrosse, J.K.; Yoshida, M.; Kato, D.;

Fujii, S.; Wordeman, M.R.; Poehmueller, P.; Parke, S.A.; Asao, Y.;

Solid-State Circuits, IEEE Journal of , Volume: 31 , Issue: 4 , April 1996

Pages:558 - 566

[\[Abstract\]](#) [\[PDF Full-Text \(1812 KB\)\]](#) IEEE JNL

8 Generation of minimal vertex covers for row/column allocation in self-repairable arrays

Smith, M.D.; Mazumder, P.;

Computers, IEEE Transactions on , Volume: 45 , Issue: 1 , Jan. 1996

Pages:109 - 115

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9 High-speed, high-reliability circuit design for megabit DRAM

Gillingham, P.; Foss, R.C.; Lines, V.; Shimokura, G.; Wojcicki, T.;

Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 8 , Aug. 1991

Pages:1171 - 1175

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) IEEE JNL

10 A 780 MHz PowerPC™ microprocessor with integrated L2 cache

Bearden, D.R.; Caffo, D.G.; Anderson, P.; Rossbach, P.; Iyengar, N.; Peterser T.A.; Jen-Tien Yen;

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12 Repair of memory arrays by cutting

Park, N.; Lombardi, E.;

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13 A 220 mm² 4 and 8 bank 256 Mb SDRAM with single-sided stitched architecture

Kirihata, T.; Gall, M.; Hosokawa, K.; Dortu, J.-M.; Wong, H.; Pfefferl, K.-P.; Ji Weinfurtnner, O.; DeBrosse, J.; Terletzki, H.; Selz, M.; Ellis, W.; Wordeman, M Kiehl, O.;

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14 A 3.3 V 16 Mb flash memory with advanced write automation

Baker, A.; Alexis, R.; Bell, S.; Dalvi, V.; Durante, R.; Baer, E.; Fandrich, M.; Jungroth, O.; Kreifels, J.; Landgraf, M.; Lee, K.; Pon, H.; Rashid, M.; Rozman, Tsang, J.; Underwood, K.; Yarlagadda, C.;

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15 Design rule centring for row redundant content addressable memo

Noghani, W.B.; Jalowiecki, I.P.;

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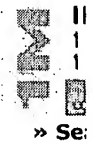
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redundancy <and> column <and> row

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1 Phase aberration correction using near-field signal redundancy-two dimensional array algorithm [medical ultrasound]

Yue Li; Robinson, B.;

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Pages:1729 - 1733 vol.2

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2 Diagnosis and repair of memory with coupling faults

Chang, M.-F.; Fuchs, W.K.; Patel, J.H.;

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3 Combined Huffman code, row and column array code and phase/frequency modulation

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Campardo, G.; Micheloni, R.; Commodaro, S.; Yero, E.; Zammattio, M.; Mogni, S.; Sacco, A.; Picca, M.; Manstretta, A.; Scotti, M.; Motta, I.; Golla, C.; Pierin, Bez, R.; Grossi, A.; Modelli, A.; Visconti, A.; Khouri, O.; Torelli, G.;

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5 New approaches for the repairs of memories with redundancy by row/column deletion for yield enhancement

Wei Kang Huang; Yi-Nan Shen; Lombardi, F.;

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Pages:1476 - 1479 vol.2

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Uphaus, J.A., Jr.; Bryant, R.B.;

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Pages:659 - 666 vol.2

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11 A 220-mm², four- and eight-bank, 256-Mb SDRAM with single-sided

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Pages:1711 - 1719

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15 High-speed, high-reliability circuit design for megabit DRAM

Gillingham, P.; Foss, R.C.; Lines, V.; Shimokura, G.; Wojcicki, T.;

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☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 A simulator for evaluating redundancy analysis algorithms of repair: embedded memories***Rei-Fu Huang; Jin-Fu Li; Jen-Chieh Yeh; Cheng-Wen Wu;*

On-Line Testing Workshop, 2002. Proceedings of the Eighth IEEE International Workshop on , 10-12 July 2002

Pages:262 - 267

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3 Balanced redundancy utilization in embedded memory cores for dependable systems*Choi, M.; Park, N.; Lombardi, F.; Kim, Y.B.; Piuri, V.;*

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McPartland, R.J.; Loeper, D.J.; Higgins, F.P.; Singh, R.; MacDonald, G.; Komo G.; Aymeloglu, S.; DePaolis, M.V.; Leung, C.W.;
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6 Integration of SRAM redundancy into production test

Jayabalan, J.; Povazanec, J.;
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8 An approach for evaluation of redundancy analysis algorithms

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9 Memory built-in self-repair using redundant words

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11 A defect-tolerant word-oriented static RAM with built-in self-test and self-reconfiguration

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Zorian, Y.;

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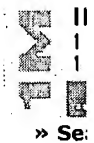
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<sentence> column) <and>
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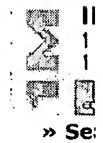
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(self <phrase> test))
<phrase> (method <or> process
<or> procedure)) <and>
```

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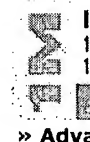
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1 A 3.3-V 12 ns 16 Mb CMOS SRAM

Goto, H.; Ohkubo, H.; Kondou, K.; Ohkawa, M.; Mitani, H.; Horiba, S.-I.; Soe M.; Hayashi, F.; Hachiya, Y.; Shimizu, T.; Ando, M.; Matsuda, Z.; Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC 1992 IEEE International , 19-21 Feb. 1992
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[Abstract] [PDF Full-Text (204 KB)] IEEE CNF

2 Built in self repair for embedded high density SRAM

Ilyoung Kim; Zorian, Y.; Komoriya, G.; Pham, H.; Higgins, F.P.; Lewandowski,
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:1112 - 1119

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memory) <and> ((bist <or>
self-test <or> (self <phrase>
test)) <phrase> (method <or>
```


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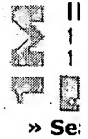
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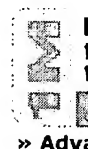
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(self <phrase> test))
<phrase> (method <or> process
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(sram <or> ram <or> dram <or>
memory) <and> (bist <or> self-
test <or> (self <phrase>
test)) <and> ((redundant <or>
```


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McPartland, R.J.; Loeper, D.J.; Higgins, F.P.; Singh, R.; MacDonald, G.; Komo G.; Aymeloglu, S.; DePaolis, M.V.; Leung, C.W.;
 Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
 Pages:287 - 289

[\[Abstract\]](#) [\[PDF Full-Text \(240 KB\)\]](#) **IEEE CNF**
2 A 3.3-V 12 ns 16 Mb CMOS SRAM

Goto, H.; Ohkubo, H.; Kondou, K.; Ohkawa, M.; Mitani, H.; Horiba, S.-I.; Soe M.; Hayashi, F.; Hachiya, Y.; Shimizu, T.; Ando, M.; Matsuda, Z.;
 Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC 1992 IEEE International , 19-21 Feb. 1992
 Pages:216 - 217, 288

[\[Abstract\]](#) [\[PDF Full-Text \(204 KB\)\]](#) **IEEE CNF**
3 Built in self repair for embedded high density SRAM

Ilyoung Kim; Zorian, Y.; Komoriya, G.; Pham, H.; Higgins, F.P.; Lewandowski,
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And 

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- 1 A new column redundancy scheme for fast access time of 64-Mb DR.**
Jun, Y.-H.; Jeong, W.-H.; Park, J.-H.; Kim, T.-H.; Kim, S.-W.; Lee, J.-S.; Jang J.; Khang, C.-M.; Lee, H.-G.;
 Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium
 on , 3-6 May 1993
 Pages:1937 - 1940 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(264 KB\)\]](#) **IEEE CNF**

- 2 A 1.6-GByte/s DRAM with flexible mapping redundancy technique and an additional refresh scheme**
Takase, S.; Kushiyama, N.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 11 , Nov. 1999
Pages:1600 - 1606

[Abstract] [PDF Full-Text (404 KB)] IEEE JNL

- 3 A flexible redundancy technique for high-density DRAMs**
Horiguchi, M.; Etoh, J.; Aoki, M.; Itoh, K.; Matsumoto, T.;
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 1 , Jan. 1991
Pages:12 - 17

[\[Abstract\]](#) [\[PDF Full-Text \(508 KB\)\]](#) **IEEE JNL**

- 4 Column redundancy scheme for multiple I/O DRAM using mapping t**
Yong-Weon Jeon; Young-Hyun Jun; Suki Kim;
 Electronics Letters , Volume: 36 , Issue: 11 , 25 May 2000
 Pages:940 - 942

[Abstract] [PDF Full-Text (481 KB)] IEE JNL

5 0.13- μ m 32-Mb/64-Mb embedded DRAM core with high efficient redundancy and enhanced testability

Kikukawa, H.; Tomishima, S.; Tsuji, T.; Kawasaki, T.; Sakamoto, S.; Ishikawa, Abe, W.; Tanizaki, H.; Kato, H.; Uchikoba, T.; Inokuchi, T.; Senoh, M.; Fukus, Y.; Nirro, M.; Maruta, M.; Shibayama, A.; Ooishi, T.; Takahashi, K.; Hidaka, H.
Solid-State Circuits, IEEE Journal of , Volume: 37 , Issue: 7 , July 2002
Pages:932 - 940

[[Abstract](#)] [[PDF Full-Text \(389 KB\)](#)] IEEE JNL

6 Dynamically shift-switched dataline redundancy suitable for DRAM macro with wide data bus

Namekawa, T.; Miyano, S.; Fukuda, R.; Haga, R.; Wada, O.; Banba, H.; Take, S.; Suda, K.; Mimoto, K.; Yamaguchi, S.; Ohkubo, T.; Takato, H.; Numata, K.
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 5 , May 2000
Pages:705 - 712

[[Abstract](#)] [[PDF Full-Text \(440 KB\)](#)] IEEE JNL

7 SEU-hardened silicon bipolar and GaAs MESFET SRAM cells using loc redundancy techniques

Hauser, J.R.;
Nuclear Science, IEEE Transactions on , Volume: 39 , Issue: 1 , Feb. 1992
Pages:2 - 6

[[Abstract](#)] [[PDF Full-Text \(396 KB\)](#)] IEEE JNL

8 Optimized redundancy selection based on failure-related yield mode 64-Mb DRAM and beyond

Kikuda, S.; Miyamoto, H.; Mori, S.; Niir, M.; Yamada, M.;
Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 11 , Nov. 1991
Pages:1550 - 1555

[[Abstract](#)] [[PDF Full-Text \(576 KB\)](#)] IEEE JNL

9 SRAM embedded memory with low cost, flash EEPROM-switch-contr redundancy

McPartland, R.J.; Loeper, D.J.; Higgins, F.P.; Singh, R.; MacDonald, G.; Komo, G.; Aymeloglu, S.; DePaolis, M.V.; Leung, C.W.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
Pages:287 - 289

[[Abstract](#)] [[PDF Full-Text \(240 KB\)](#)] IEEE CNF

10 Integration of SRAM redundancy into production test

Jayabalan, J.; Povazanec, J.;
Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002
Pages:187 - 193

[[Abstract](#)] [[PDF Full-Text \(426 KB\)](#)] IEEE CNF

11 Dynamically shift-switched dataline redundancy suitable for DRAM macro with wide data bus

Namekawa, T.; Miyano, S.; Fukuda, R.; Haga, R.; Wada, O.; Banba, H.; Take, S.; Suda, K.; Mimoto, K.; Yamaguchi, S.; Ohkubo, T.; Takato, H.; Numata, K.
VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on , 17-19 : 1999

Pages:149 - 152

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) [IEEE CNF](#)

12 A 1.6 GB/s DRAM with flexible mapping redundancy technique and additional refresh scheme

Takase, S.; Kushiya, N.;
Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International , 15-17 Feb. 1999

Pages:410 - 411

[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) [IEEE CNF](#)

13 A defect and fault tolerant design of WSI static RAM modules

Tsuda, N.;
Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 23-25 Jan. 1990

Pages:213 - 219

[\[Abstract\]](#) [\[PDF Full-Text \(288 KB\)\]](#) [IEEE CNF](#)

14 I/O divided column redundancy scheme for high-speed DRAM with multiple I/Os

Jae-Goo Lee; Young-Hyun Jun; Chilgee Lee; Bai-Sun Kong;
Electronics Letters , Volume: 36 , Issue: 24 , 23 Nov 2000

Pages:1996 - 1997

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) [IEEE JNL](#)

15 Redundancy techniques for high-density DRAMs

Horiguchi, M.;
Innovative Systems in Silicon, 1997. Proceedings., Second Annual IEEE International Conference on , 8-10 Oct. 1997

Pages:22 - 29

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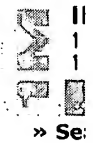
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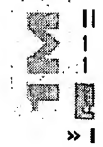
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On-Line Testing Workshop, 2000. Proceedings. 6th IEEE International , 3-5 Ju 2000

Pages:214 - 218

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) IEEE CNF
2 Diagonal test and diagnostic schemes for flash memories*Sau-Kwo Chiu; Jen-Chieh Yeh; Chih-Tsun Huang; Cheng-Wen Wu;*

Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002

Pages:37 - 46

[\[Abstract\]](#) [\[PDF Full-Text \(515 KB\)\]](#) IEEE CNF
3 GRAAL: a tool for highly dependable SRAMs generation*Chiusano, S.; Di Natale, G.; Prinetto, P.; Bigongiari, F.;*

Test Conference, 2001. Proceedings. International , 30 Oct.-1 Nov. 2001

Pages:250 - 257

[\[Abstract\]](#) [\[PDF Full-Text \(754 KB\)\]](#) IEEE CNF
4 R-CBIST: an effective RAM-based input vector monitoring concurrent BIST technique*Voyiatzis, I.; Paschalis, A.; Nikolos, D.; Halatsis, C.;*

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998

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